AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A multi-chip integrated module, comprising:

a transparent substrate, which has a circuit layer formed directly on one surface of the transparent substrate, wherein the circuit layer formed on the surface of the transparent substrate comprises a circuit for electrical inter-connection and a plurality of electrical pads;

at least two chips, which are respectively mounted on the transparent substrate by way of a flip-chip bonding, wherein the chips and the circuit for electrical inter-connection construct a circuit system; and

a circuit substrate, which attaches to the transparent substrate, and at least comprises a circuit layer of the circuit substrate, wherein the electrical pads of the transparent substrate electrically connect to the circuit layer of the circuit substrate.,

wherein at least one gap is located between the chips and the circuit substrate.

2. (Original) The multi-chip integrated module of claim 1, wherein the transparent substrate is a glass substrate.

3. (Previously Presented) The multi-chip integrated module of claim 1, wherein a plurality of first bumps are formed on the electrical pads of the transparent substrate, respectively, for electrically connecting the electrical pads and the circuit layer of the circuit substrate.

4. (Previously Presented) The multi-chip integrated module of claim 1, wherein a plurality of second bumps are formed on a part of the circuit for electrical inter-connection, and the chips electrically connect to the second bumps by way of a flip-chip bonding.

Claims 5-8 (Cancelled)

9. (Currently Amended) The multi-chip integrated module of ~~claim 8~~ claim 1, wherein a heat dissipation element is formed on the backside of at least one of the chips.

10. (Original) The multi-chip integrated module of claim 1, wherein the circuit substrate is a printed circuit substrate.

11. (Original) The multi-chip integrated module of claim 1, further comprising: a passive component, which is formed on the transparent substrate and electrically connects to the circuit for electrical inter-connection on the transparent substrate.

12. (Original) The multi-chip integrated module of claim 1, further comprising: an active component, which is formed on the transparent substrate and electrically connects to the circuit for electrical inter-connection on the transparent substrate.

13. (Currently Amended) A multi-chip integrated module, comprising:

a transparent substrate, which has a circuit layer formed directly on one surface of the transparent substrate, wherein the circuit layer formed on the surface of the transparent substrate comprises a circuit for electrical inter-connection, ~~and~~ a plurality of second bumps ~~are~~ formed on a part of the circuit for electrical ~~inter-connection;~~ inter-connection, a plurality of electrical pads for electrical external-connection, and a plurality of first bumps formed on the electrical pads, respectively; and

at least two chips, which electrically connect to the bumps of the circuit for electrical inter-connection by way of a flip-chip bonding, wherein the chips and the circuit for electrical inter-connection construct a circuit system[[.]],

wherein the height of the first bumps are larger then the height of the chips.

14. (Canceled)

15. (Original) The multi-chip integrated module of claim 13, wherein the transparent substrate is a glass substrate.

16. (Previously Presented) The multi-chip integrated module of claim 13, wherein the second bumps are solder bumps or gold bumps.

Claims 17-18 (Cancelled)

19. (Original) The multi-chip integrated module of claim 13, further comprising: a passive component, which is formed on the transparent substrate and electrically connects to the circuit for electrical inter-connection on the transparent substrate.

20. (Original) The multi-chip integrated module of claim 13, further comprising: an active component, which is formed on the transparent substrate and electrically connects to the circuit for electrical inter-connection on the transparent substrate.

21. (Currently Amended) A multi-chip integrated module, comprising:

a transparent substrate, which has a circuit layer formed directly on one surface of the transparent substrate, wherein the circuit layer formed on the surface of the transparent substrate comprises a circuit for electrical inter-connection and a plurality of electrical pads;

at least two chips, which are respectively mounted on the transparent substrate by way of a flip-chip bonding, wherein the chips and the circuit for electrical inter-connection construct a circuit system; and

a circuit substrate, which attaches to the transparent substrate, and at least comprises a circuit layer of the circuit substrate, wherein the electrical pads of the transparent substrate electrically connect to the circuit layer of the circuit substrate, the circuit substrate has a hollow portion, and when the circuit substrate attaches to the transparent substrate, the chips are positioned in the hollow portion of the circuit substrate[[.]],

<u>wherein at least one gap is located between the chips and the circuit substrate.</u>

22. (Previously Presented) The multi-chip integrated module of claim 21, wherein the transparent substrate is a glass substrate.

23. (Previously Presented) The multi-chip integrated module of claim 21, wherein a plurality of first bumps are formed on the electrical pads of the transparent substrate, respectively, for electrically connecting the electrical pads and the circuit layer of the circuit substrate.

24. (Previously Presented) The multi-chip integrated module of claim 21, wherein a plurality of second bumps are formed on a part of the circuit for electrical inter-connection, and the chips electrically connect to the second bumps by way of a flip-chip bonding.

25. (Previously Presented) The multi-chip integrated module of claim 21, wherein a heat dissipation element is formed on the backside of at least one of the chips.

26. (Previously Presented) The multi-chip integrated module of claim 21, wherein the circuit substrate is a printed circuit substrate.